**What is claimed is:**

1. A bit string check method including a process of checking against a plurality of bit patterns registered in advance at multiple stages with dividing a bit string to be searched into a plurality of partial-object bit strings,

wherein a current stage being one check stage included in the multiple stages, comprising:

an all-check step of selecting a partial-object bit string of the current stage from the bit string to be searched and comparing the partial-object bit string of the current stage with all possible values of a partial-object bit string of the current stage;

a pattern loading step of loading a pattern table of the current stage from a memory **independently of the all-check step** before, after or in parallel with the all-check step, the pattern table being for indicating a partial registration bit pattern of each of the plurality of registration bit patterns, **the pattern table having a range corresponding to all possible values of a partial-object bit string of the current stage,** the pattern table being determined by check-continuation information received from a stage preceding the current stage;

a judgment step of obtaining a check result indicating at least a presence or absence of the partial registration bit pattern of the current stage which matches the partial-object bit string of the current stage in accordance with the result of the all-check step and the pattern table of

the current stage; and

an outputting step of outputting check-continuation information including the address of a pattern table of the stage subsequent to the current stage from an address table corresponding to the pattern table of the current stage in accordance with the check result.

2. The check method according to claim 1, wherein the pattern table is mask data consisted of a bit flag indicating a validness or invalidness of the partial registration bit pattern.

3. The check method according to claim 1, wherein the outputting step outputs check-continuation information including the address of a pattern table of the next stage subsequent to the matched partial registration bit patterns of the current stage.

4. The check method according to claim 1,

wherein the check result of the judgment step further includes a presence or absence of a partial registration bit pattern having the maximum or minimum value closest to the partial-object bit string in the current stage, and

wherein the check-continuation information of the outputting step further includes an address of a scope

search pattern table of the next stage subsequent to the maximum or minimum partial registration bit pattern of the current stage.

5. The check method according to claim 4, further comprising a candidate address storing step of storing the address of the scope search pattern table when the matched partial registration bit pattern of the current stage is present and when the maximum or minimum partial registration bit pattern of the current stage is present,

wherein the check-continuation information of the outputting step further includes the candidate address when the matched partial registration bit pattern of the current stage is not present and when the maximum or minimum partial registration bit pattern of the current stage is not present.

6. The check method according to claim 4, further comprising a step of bypassing the all-check step and the judgment step when the check-continuation information including the address of the scope search pattern table is given,

wherein the check-continuation information of the outputting step further includes the address of the pattern table of the next stage subsequent to the maximum or minimum partial registration bit pattern shown on the pattern table,

from the address table corresponding to the scope search pattern table.

7. The check method according to claim 4,

wherein the pattern table further includes bypass data indicating the maximum or minimum registration bit pattern determined in correspondence with the maximum or minimum partial registration bit pattern shown on the pattern table,

wherein the check method further comprises the step of bypassing the all-check step, the pattern loading step, and the judgment step when the check-continuation information including the address of the scope search pattern table is given, and

wherein the outputting step outputs the final check information including the bypass data corresponding to the scope search pattern table to terminate the check of the bit string to be searched.

8. The check method according to claim 1, further comprising an updating step of adding or deleting a registration bit pattern by updating the pattern table and the address table.

9. The check method according to claim 1, wherein the all-check step and the pattern loading step are executed in

parallel.

10. The check method according to claim 1, wherein a plurality of the check stages are executed in a pipeline.

11. The check method according to claim 10, further comprising an updating step of adding or deleting a registration bit pattern by updating a check table including the pattern table and the address table of each of the check stages, the updating step being executed in a pipeline in parallel to the check stage.

12. The check method according to claim 11,

wherein the check table further includes bypass data indicating the maximum or minimum registration bit pattern determined in correspondence with the maximum or minimum partial registration bit pattern shown on the pattern table, and

wherein the updating step updates the lower order check table of the check stage from the upper order check table of the check stage with the exception that the updating of the check table of the check stage having a possibility of updating the bypass data is executed after awaiting the updating of the lower order check table of the check stage.

13. The check method according to claim 11,

wherein the check table further includes bypass data indicating the maximum or minimum registration bit pattern determined in correspondence with the maximum or minimum partial registration bit pattern shown on the pattern table, and

wherein the updating step includes:

a step of updating the lower order check table of the check stage from the upper order check table of the check stage; and

a step of updating upper order check table with a bidirectional link when the updating of the bypass data of the upper order check table is generated by updating of the lower order check table.

14. The check method according to claim 1, wherein data including the check-continuation information is packetized and transmitted between the plurality of check stages.

15. A classification method, comprising:

a classification process including the plurality of check stages of claim 4,

wherein the registration bit pattern indicates a scope

including a plurality of classification results.

16. The check method according to claim 15, further comprising:

the plurality of classification processes; and

a logical operation process for performing a logical AND of the plurality of classification results included in a plurality of scopes obtained through the plurality of classification processes to obtain a final classification result.

17. The check method according to claim 16, wherein the logical operation process performs a matrix operation of the logical AND of the plurality of classification results to obtain the final classification result.

18. A data management method, comprising the steps of:

checking the scope to which the bit string to be searched belongs by the classification method of claim 15, with regarding a bit string to manage a packet including at least one of an IP address, a port number, and a protocol as the bit string to be searched; and

managing the packet including the bit string to be searched on the basis of the classification result of the scope to which the bit string to be searched belongs.

19. A data management method, comprising the steps of:

checking the bit string to be searched by the checking method of claim 1; and

managing data including the bit string to be searched on the basis of a checking result of the checking step.

20. A control method of a data processing device, comprising:

a step of checking by the checking method of claim 1 with regarding data forming an evaluation source of a state transition as the bit string to be searched, and with regarding data indicating a plurality of state transition conditions as the plurality of registration bit patterns; and

a step of transiting states of a data processing circuit in accordance with a check result of the check step.

21. A check device for executing at lease one stage included in multiple stages so as to check against a plurality of bit patterns registered in advance at the multiple stages with dividing a bit string to be searched into a plurality of partial-object bit strings, the check device comprising:

all-check means for selecting a partial-object bit

string of the current stage from the bit string to be searched and for comparing the partial-object bit string of the current stage with all possible values of a partial-object bit string of the current stage;

pattern loading means for loading a pattern table of the current stage from a memory **independently of the all-check means**, the pattern table being for indicating a partial registration bit pattern of each of the plurality of registration bit patterns, **the pattern table having a range corresponding to all possible values of a partial-object bit string of the current stage**, the pattern table being determined by check-continuation information received from a stage preceding the current stage;

judgment means for obtaining a check result indicating at least a presence or absence of the partial registration bit pattern of the current stage which matches the partial-object bit string of the current stage in accordance with the result of the all-check means and the pattern table of the current stage; and

outputting means for outputting check-continuation information including the address of a pattern table of the stage subsequent to the current stage from an address table corresponding to the pattern table of the current stage in accordance with the check result.

22. The check device according to claim 21, wherein the pattern table is mask data consisted of a bit flag indicating a validness or invalidness of the partial

registration bit pattern.

23. The check device according to claim 21, wherein the outputting means outputs check-continuation information including the address of a pattern table of the next stage subsequent to the matched partial registration bit patterns of the current stage.

24. The check device according to claim 21,

wherein the check result outputted from the judgment means further includes a presence or absence of a partial registration bit pattern having the maximum or minimum value closest to the partial-object bit string in the current stage, and

wherein the check-continuation information outputted from the outputting means further includes an address of a scope search pattern table of the next stage subsequent to the maximum or minimum partial registration bit pattern of the current stage.

25. The check device according to claim 24,

wherein the outputting means further outputs the address of the scope search pattern table as a candidate address when the matched partial registration bit pattern of the current stage is present and when the maximum or minimum

partial registration bit pattern of the current stage is present, and

outputs the check-continuation information including the candidate address when the matched partial registration bit pattern of the current stage is not present and when the maximum or minimum partial registration bit pattern of the current stage is not present.

26. The check device according to claim 24,

wherein the outputting means outputs, when the check-continuation information including the address of the scope search pattern table is given, the check-continuation information including the address of the pattern table of the next stage subsequent to the maximum or minimum partial registration bit pattern shown on the pattern table, from the address table corresponding to the scope search pattern table.

27. The check device according to claim 24,

wherein the pattern table further includes bypass data indicating the maximum or minimum registration bit pattern determined in correspondence with the maximum or minimum partial registration bit pattern shown on the pattern table, and

wherein the outputting means outputs, when the check-

continuation information including the address of the scope search pattern table is given, the bypass data corresponding to the scope search pattern table as final check information.

28. The check device according to claim 21, further comprising an updating means for adding or deleting a registration bit pattern by updating the pattern table and the address table.

29. The check device according to claim 21, wherein the all-check means and the pattern loading means operates in parallel.

30. A classification device comprising a plurality of the check stages of claim 21.

31. The classification device according to claim 30, wherein the plurality of check stages are coupled in a pipeline.

32. The classification device according to claim 30, wherein data including the check-continuation information is packetized and propagated between the plurality of check devices.

33. The classification device according to claim 30, further comprising a cash device for inputting and outputting data from and to the memory.

34. The classification device according to claim 33, wherein the memory stores a check table including the pattern table and the address table, and the size of a cache line of the cash device is equal to the size of the check table.

35. The classification device according to claim 34, further comprising a unit for receiving information of search types designating the first check table, and wherein the cache device comprises a management unit for allocating the cache line in a unit of each of types to be searched and the check device, and managing the cache line in a unit of each of types to be searched and the check device.

36. The classification device according to claim 34, further comprising means for receiving search type information designating a first check table,

wherein the check table is stored in an individual address range allocated in a unit of each search type and each check stage, in the memory and

wherein a cache line of the cache device is allocated

in a unit of the individual address range.

37. The classification device according to claim 33, wherein, when the check table is not an on-cache, the cache device informs this to the check device, stops the process of the check device and returns to a queue.

38. The classification device according to claim 30, further comprising a history cache device, for storing a classification result of the corresponding classification device, comparing the classification result of the corresponding classification device with the bit string to be searched before providing the bit string to be searched to the check device.

39. A search device comprising a classification device of claim 30, wherein the registration bit pattern indicates a scope including a plurality of classification results, wherein the search device outputs a classification result to which the bit string to be searched belongs.

40. The search device according to claim 39, further comprising:

a plurality of the classification devices; and

a logical operation device for operating a logical AND

of a plurality of classification results included in the plurality of scopes obtained by the plurality of classification devices to obtain the final classification result.

41. The search device according to claim 40, wherein the logical operation device performs a matrix operation of the logical AND of the plurality of classification results to obtain the final classification result.

42. The search device according to claim 39, further comprising a cache device for inputting and outputting data from and to a memory.

43. The search device according to claim 39, further comprising a history cache device, for storing a search result of the corresponding searching device, comparing the search result of the corresponding search device with the bit string to be searched before providing the bit string to be searched to the classification device.

44. A data managing device, comprising:

the search device of claim 40;

means for providing a bit string for managing a packet including at least one of an IP address, a port number, and

a protocol as a bit string to be searched, to the search device; and

means for managing the packet including the bit string to be searched on the basis of a classification result outputted from the search device.

45. A data managing device, comprising:

the classification device of claim 30; and

means for managing data including the bit string to be searched on the basis of the output of the classification device.

46. A data processing device, comprising:

the classification device of claim 30, wherein the plurality of registration bit patterns are regarded as data indicating a plurality of state transition conditions;

searching object provision means for providing data forming an evaluation source of state transition as the bit string to be searched, to the classification device; and

a data processing circuit whose state is transited in accordance with an output of the classification device.

47. The data processing device according to claim 46,

wherein the memory stores a check table including the pattern table and the address table, and

wherein the check table provided to the first check device is determined by the output of the classification device or the searching object provision means.

48. The data processing device according to claim 47, wherein the memory stores a check table including the pattern table and the address table, and the check table of the memory is rewritten by the data processing circuit.

49. A data processing device, comprising:

a check device for checking a bit string to be searched of a current state forming an evaluation source of a state transition against a registration bit pattern indicating a plurality of state transition conditions registered in advance;

search object provision means for providing the bit string to be searched to the check device; and

a data processing circuit whose state is transited in accordance with an output of the check device,

wherein the data processing device further comprises:

all-check means for comparing all possible values of a bit string to be searched in a current stage;

pattern loading means for loading a pattern table of the current state from a memory **independently of the all-check means**, the pattern table being for indicating the plurality of registration bit pattern, **the pattern table**

**having a range corresponding to all possible values of a partial-object bit string of the current stage,** the pattern table being determined by check-continuation information obtained from a preceding stage;

judgment means for outputting a check result indicating at least a presence or absence of the registration bit pattern of the current state which matches the bit string to be searched of the current state in accordance with the result of the all-check means and the pattern table of the current state of the all-check means; and

outputting means for outputting check-continuation information including the address of the pattern table of the next state subsequent to the current state in accordance with the check result.

50. The data processing device according to claim 49, wherein the memory stores a check table including the pattern table and the address table, and the check table provided to the check device is determined by the searching object provision means.

51. The data processing device according to claim 49, wherein the memory stores a check table including the pattern table and the address table, and the check table of the memory is rewritten by the data processing circuit.

52. The check method according to claim 1, wherein, in the all-check step, the check is performed by hardware employing a comparator or a look-up table. (16)

53. The check device according to claim 21, wherein the all-check means performs the check with hardware employing a comparator or a look-up table. (17)

54. The data processing device according to claim 49, wherein the all-check means performs the check with hardware employing a comparator or a look-up table. (18)